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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,182	03/19/2004	Rino Micheloni	2110-108-3	7411

7590 05/27/2009

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EXAMINER	
MANOSKEY, JOSEPH D	

ART UNIT	PAPER NUMBER
2113	

MAIL DATE	DELIVERY MODE
05/27/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/805,182	MICHELONI ET AL.	
	Examiner	Art Unit	
	JOSEPH D. MANOSKEY	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 an 9-21* is/are rejected.

7)☒ Claim(s) *4-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3 and 9-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Longwell, et al. U.S. Patent 7,134,069, hereinafter referred to as "Longwell".

3. Referring to claim 1, Longwell teaches a memory system with integrated circuits such as DRAM (See Fig. 1, Col. 1, lines 5-8 and Col. 3, lines 38-40). This is interpreted as an integrated memory system, comprising: a non-volatile solid-state memory. Longwell teaches error detection and correction (EDAC) units that includes both word-wise error detection and correction (WEDAC) units and bit-wise error detection and correction (BEDAC) units (See Col. 3, lines 15-37). The BEDAC unit is capable of correcting double-bit errors which the WEDAC is not capable of doing (See Col. 3, lines 15-37). This is interpreted as an automatic storage error corrector including functionally independent devices, each device to correct a different predetermined storage error of

data stored in the memory. Longwell also teaches the EDAC units are separate from the DRAM array (See Fig. 1). This interpreted as at least one of said devices being external to the memory.

4. Referring to claim 2, Longwell teaches the use of memory controller connected to the data bus and the EDAC units (See Fig. 1). This is interpreted as wherein said memory is connected to a controller by means of an interface bus and said devices are incorporated both in the memory and in the controller.

5. Referring to claim 3, Longwell teaches BEDAC unit is capable of correcting double-bit errors which the WEDAC is not capable of doing (See Col. 3, lines 15-37). The WEDAC does single bit detection and correction (See Col. 5, lines 7-31). Longwell also teaches the use of a syndrome calculator (See Col. 9, lines 47-52). This is interpreted as including coding circuits to correct two errors, a logic to calculate a syndrome, a single error correcting circuit, and a logic to detect more than one error.

6. Referring to claim 9, Longwell teaches a memory system with integrated circuits such as DRAM (See Fig. 1, Col. 1, lines 5-8 and Col. 3, lines 38-40). Longwell teaches error detection and correction (EDAC) units that includes both word-wise error detection and correction (WEDAC) units and bit-wise error detection and correction (BEDAC) units (See Col. 3, lines 15-37). The BEDAC unit is capable of correcting double-bit errors which the WEDAC is not capable of doing (See Col. 3, lines 15-37). This is

interpreted as a system, comprising: a first circuit operable to store data in a non-volatile solid-state memory, the data having associated therewith at least one storage error of a plurality of storage-error types, the first circuit operable to correct a first-type error of the plurality of storage-error types; and a second circuit coupled to the first circuit, the second circuit operable to correct a second-type error of the plurality of storage-error types.

7. Referring to claim 10, Longwell teaches using stack-wise error detection and correction (See Col. 13, line 64 to Col. 14, line 15). This is interpreted as wherein the second circuit to generate a signal requesting correction of a third-type error of the plurality of storage-error types.

8. Referring to claim 11, Longwell also teaches the use of a syndrome calculator (See Col. 9, lines 47-52). This is interpreted as wherein the first circuit further to determine at least one syndrome associated with the at least one storage error.

9. Referring to claim 12, Longwell teaches the WEDAC detecting errors (See Col. 5, lines 7-31). This is interpreted as wherein the first circuit further to detect the second-type error.

10. Referring to claim 13, Longwell teaches the BEDAC unit is capable of correcting double-bit errors which the WEDAC is not capable of doing (See Col. 3, lines 15-37).

This is interpreted as wherein the second circuit to correct the second-type error in response to a signal generated by the first circuit.

11. Referring to claim 14, Longwell teaches a memory system with integrated circuits such as DRAM (See Fig. 1, Col. 1, lines 5-8 and Col. 3, lines 38-40). This is interpreted as wherein the first circuit comprises a non-volatile memory.

12. Referring to claim 15, Longwell teaches the WEDAC and BEDAC being separate circuits (See Fig.1). This is interpreted as wherein: the first circuit is disposed on a first integrated circuit; and the second circuit is disposed on a second integrated circuit.

13. Referring to claim 16, Longwell teaches the system containing circuits See Fig. 1, Col. 1, lines 5-8 and Col. 3, lines 38-40). This is interpreted as wherein the first and second circuits are disposed on an integrated circuit.

14. Referring to claim 17, Longwell teaches a memory system with integrated circuits such as DRAM (See Fig. 1, Col. 1, lines 5-8 and Col. 3, lines 38-40). Longwell teaches error detection and correction (EDAC) units that includes both word-wise error detection and correction (WEDAC) units and bit-wise error detection and correction (BEDAC) units (See Col. 3, lines 15-37). The BEDAC unit is capable of correcting double-bit errors which the WEDAC is not capable of doing (See Col. 3, lines 15-37). This is interpreted as a memory device, comprising: a non-volatile solid-state storage portion to

store data having associated therewith at least one storage error of a plurality of storage-error types; a first circuit to correct a first-type error of the plurality of storage-error types; and a second circuit to generate a signal indicating detection of a second-type error of the plurality of storage-error types.

15. Referring to claim 18, Longwell teaches using stack-wise error detection and correction (See Col. 13, line 64 to Col. 14, line 15). Longwell also teaches the use of a syndrome calculator (See Col. 9, lines 47-52). This is interpreted as further comprising a third circuit to determine at least one syndrome associated with the at least one storage error.

16. Referring to claim 19 and 20, Longwell teaches a memory system with integrated circuits such as DRAM (See Fig. 1, Col. 1, lines 5-8 and Col. 3, lines 38-40). Longwell teaches error detection and correction (EDAC) units that includes both word-wise error detection and correction (WEDAC) units and bit-wise error detection and correction (BEDAC) units (See Col. 3, lines 15-37). The BEDAC unit is capable of correcting double-bit errors which the WEDAC is not capable of doing (See Col. 3, lines 15-37). This is interpreted as a method, comprising: storing, in a non-volatile solid-state memory location of a device, data having associated therewith at least one storage error of a plurality of storage-error types; and correcting, at the memory location, a first-type error of the plurality of storage-error types. This is also interpreted as further comprising

generating, at the memory location, an interrupt-request signal indicating detection of a second-type error of the plurality of storage-error types.

17. Referring to claim 21, Longwell teaches a memory system with integrated circuits such as DRAM (See Fig. 1, Col. 1, lines 5-8 and Col. 3, lines 38-40). Longwell teaches error detection and correction (EDAC) units that includes both word-wise error detection and correction (WEDAC) units and bit-wise error detection and correction (BEDAC) units (See Col. 3, lines 15-37). The BEDAC unit is capable of correcting double-bit errors which the WEDAC is not capable of doing (See Col. 3, lines 15-37). This is interpreted as an electronic system, comprising: a first integrated circuit having a non-volatile solid-state memory to store data having associated therewith at least one storage error of a plurality of storage-error types, the memory to correct a first-type error of the plurality of storage-error types; and a second integrated circuit coupled to the first circuit, the second integrated circuit having processor to correct a second-type error of the plurality of storage-error types.

Allowable Subject Matter

18. Claims 4-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

19. Applicant's arguments, see pages 1 and 2 of pre-appeal brief, filed 04 March 2009, with respect to the rejection(s) of claim(s) 1-21 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of new found prior art, see above rejections.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following are closely related memory systems.

U.S. Patent 6,802,040 to Ohyama et al.

U.S. Patent App. Pub. 2002/0174397 to Furukawa

U.S. Patent App. Pub. 2003/0126513 to Wuidart

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH D. MANOSKEY whose telephone number is (571)272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDM
May 22, 2009

/Robert W. Beausoliel, Jr./
Supervisory Patent Examiner, Art Unit 2113